[0048]

The present invention is a combination of one dot 256 grades output from power modulation of laser diode and two dots matrix in the main scanning direction and counter scanning direction. Figure 9 (a) shows 1 × 2 matrix that performs area gradation by adjacent two dots in the counter scanning direction. Figure 9 (b) shows an optical writing method of 2 × 1 matrix for performing area gradation by adjacent two dots in the main scanning direction. In the low density part, when an exposure power is increased for one of the two dots to the maximum (255), the next dot's exposure power will be increased. In the above description, two dots in the main scanning direction or the counter scanning direction are considered one pixel of interest and density reproduction is performed. Reading density for CCD 117 is in proportion to its receiving amount of light. Therefore, the receiving amount of light for CCD 117 is linear to manuscript reflection density. Density data of two dots is added to digital value, γ conversion is performing on the added value. In this manner, conversion into writing density data is performed according to the above-mentioned method. As a result, 512 gradations can be provided by two dots in main scanning direction and counter scanning direction.

[0049]

Figure 10 is an illustration showing generating operation of a halftone density region. In Figure 10,

density is filled starting at EVEN dots. 1 × 2 matrices in Figure 10 (a), (c) where area gradation is performed in the counter scanning direction is based on a horizontal line in a sequential halftone region. 2 × 1 matrices in Figure 10 (b), (d) where area gradation is performed in the main scanning direction is based on a vertical line in a sequential halftone region.

[0050]

In figures 10 (c), (d), writing phases of Figures 10 (a), (b) are changed to the opposite direction, where a two dots line is formed in main scanning and counter scanning, resulting in an image of 100 lines. This does not change the number of grades but lines gather and resolution appears to drop by half.

[0051]

(5) Two dots multi-valued algorithm

Two dots in the main scanning direction and counter scanning direction are considered a pixel of interest and density reproduction is performed. Reading voltage of CCD 117 is in proportion to its receiving amount of light. The receiving amount of light for CCD 117 is linear to manuscript reflection density. Light amount data of two dots is added in digital value. By adding in reflection amount of light data, the sum of reflection amount of two dots is determined and the data, where two dots are considered as one pixel, is obtained. Then, γ conversion is performed on the added value to convert into writing density data. Distribution

of density data and grade correction are converted into writing density data of one pixel comprising two dots so as to make it equal to reading density of one pixel comprising two dots.

[0052]

Density conversion algorithm for two dots multi-valued writing is described as expressions below.

$F(Dm + Dm_{+1}) = Pm + Pm_{+1}$

when $Pm + Pm_{+1} < 255$, $Pm_{+1} = 0$

and when $Pm + Pm_{+1} \geq 255$, $Pm = 255$.

[0053]

In the above expressions, Dm is reading density data at m^{th} dot in the main scanning direction or the counter scanning direction, Pm is writing density data at m^{th} dot in the main scanning direction or the counter scanning direction, and F is density conversion function including γ correction. If density conversion is linear, density conversion function F is a constant, represented by 4.

[0054]

Conventional dot forming method of two dots multi-valued writing according to the above-mentioned method looks like Figure 15 as it regularly performs dots distribution of density data. Shaded area represents density generating dots and arrows show the direction in which density data transits. In 1×2 matrix shown in Figure 15 (a) and 2×1 matrix image shown in Figure 15 (b),

distribution of two dots weighting is in the same direction, each forming horizontal and vertical line images.

[0055]

In the first embodiment of the present invention, distribution of weighting begins at high density dot in manuscript information, and conversion is performed under the condition of

where $Dm \geq Dm_{+1}$,

when $Pm + Pm_{+1} < 255$, $Pm_{+1} = 0$

when $Pm + Pm_{+1} \geq 255$, $Pm = 255$,

and where $Dm < Dm_{+1}$,

when $Pm + Pm_{+1} < 255$, $Pm = 0$

when $Pm + Pm_{+1} \geq 255$, $Pm_{+1} = 255$,

, while maintaining a density of a pixel.

[0056]

In the second embodiment of the present invention, density difference in a reading dot and threshold T is compared, and conversion is performed under the condition of

where $|Dm - Dm_{+1}| < T$ or $Dm \geq Dm_{+1}$,

when $Pm + Pm_{+1} < 255$, $Pm_{+1} = 0$

when $Pm + Pm_{+1} \geq 255$, $Pm = 255$,

and where $|Dm - Dm_{+1}| \geq T$ and $Dm < Dm_{+1}$,

when $Pm + Pm_{+1} < 255$, $Pm = 0$

when $Pm + Pm_{+1} \geq 255$, $Pm_{+1} = 255$.

[0057]

(6) Two dots multi-valued circuit

Figure 11 is a block diagram showing a configuration of two dots multi-valued circuit for performing two dots multi-valued and dot phase weighing. The figure includes serially connected line memory (FIFO) 1101, 1102 for inputting a six bits signal input from a scanner, latches (D-F/F) 1103, 1104, adder 1105 connected to the line memory 1101, 1102 and latches 1103, 1104 via switches SW1-SW4, respectively, ROM 1106 connected to the adder 1105 (LUT: lookup table), and separator 1107 including a data subtracting part and a comparing part. Output from the ROM 1106 is output into a printer as an eight-bit data signal.

[0058]

In the above-mentioned configuration, two dots multi-valued writing data is formed by two dots, six-bit each, reading data and a density generating dot is switched for each pixel. A data signal delay part is provided so that a data signal and a switching signal (SEL) are synchronized. (1) 1 × 2 matrix, (2) 2 × 1 matrix, and (3) density dot generation will be described separately below.

[0059]

(1) 1 × 2 matrix

When area gradation is performed by two dots in the counter scanning direction, (1 × 2 matrix) delays reading data for two of main scanning lines with two line memory (FIFO) 1101, 1102. SW1 switch is selected from SW3, 4 and switches for each main scanning line. Then, two pieces of six-bit data are added with adder 1105, and the seven-bit

data is input into ROM 1106 for γ conversion. In ROM 1106, one table is configured by 256 bytes, and 128 bytes of the first half is EVEN data, and 128 bytes of the latter half is ODD data.

[0060]

First, the beginning addition data is input into an address bus of ROM 1106, and EVEN data, which is represented by the address of data and switching signal (SEL), is output as writing data. The same data is added in the next line, and writing data, which is represented by data and switching signal (SEL), from a data bus. Switching of EVEN (L) and ODD (H) is selected by a switching signal (SEL) and data of density generation dots is designated by EVEN.

[0061]

In the block diagram of two dots multi-valued circuit shown in Figure 11, switch SW1 and EVEN/ODD switch for each main scanning line, and switches SW3, SW4 are set to the upper side to select data from line memory 1101, 1102.

[0062]

(2) 2 × 1 matrix

When area gradation is performed by two dots in the main scanning direction, (2 × 1 matrix) uses two latches (D-F/F) 1103, 1104 and delays reading data for two dots in the main scanning direction. Then, addition and γ conversion are performed and writing data is output as in the case of 1 × 2 matrix. Then, the operation transfers to the next two dots and repeats the process sequentially. In this case,

SW2 is selected from SW3, 4 (lower part of the figure) and switches for each writing clock. No gradation information is lost in every mode.

[0063]

(3) Occurrence of density dots

Separator 1107 includes data subtraction part and comparing part. Subtraction of six-bit data is performed by taking a complement and adding it. When a target dot data is determined greater than the other data (determined that its reading density is higher than the other), data on the density generating side where a switching signal (SEL) is represented by EVEN, is designated.

[0064]

In Figure 11, obtained subtraction data ranges from 0 to 63, and the value is compared with a threshold (TH). A threshold can be input from 0 to 63, and comparison is determined by an overflow caused by adding complements of subtraction data and threshold data. As the result of the comparison, pixel with an overflow has a density difference two dots more than the set threshold. Therefore, when a target dot data is determined greater than the other data as mentioned above, a switching signal (SEL) designates dot data on the density generating side represented by EVEN. On the other hand, when the density difference is smaller than the threshold by two dots, EVEN and ODD dots are generated regularly as shown in Figure 15 (a) and (b), whether the dot data is big or small. Determination has been done in

real time based on image data and writing data has been generated.

[0065]

Figure 12 shows an example of γ conversion table of LUT (lookup table) within ROM 1106 used in the device. It is set to make a reproduced density is almost same as the manuscript density. In Figure 12, EVEN dot on one side is exposed up to middle density, increased against input data, and when the EVEN dot comes close to the maximum, exposure intensity of ODD dot is increased. This gathers dots, while maintaining density information on two dots. Generally, by making inverse conversion of γ feature of a printer represented by print density against writing exposure amount of light a table value, γ character of a single printer can be linear.

[0066]

Two dots multi-valued circuit shown in Figure 11 is arranged in IPU 800; image data for each dot from a scanner is converted and output into a writing system. As a result, writing of 512 grades can be performed with two dots unit in the main scanning direction and the counter scanning direction regarded as one pixel.

[0067]

Figure 13 shows examples of image output in conventional method and the method according to the present invention. (a) indicates vertical line image, (b) indicates a text "ア", (c) indicates a graphic pattern, while (1) indicates

a manuscript state, (2) indicates an example of output according to conventional method, and (3) indicates an example of output according to the present invention, respectively. This is the method using 2 × 1 matrix shown in Figure 15 (b). For simplifying the description, output of data is represented by dot and density is shown by the size of dot. In either case, one pixel is formed by two dot unit, though in the present invention, image is reproduced in the location more faithful to a manuscript. Particularly, it is apparent that, in an output image shown in Figure 13 (a) according to the present invention, the pitch difference is reduced in a line image of even pitch and breaking of lines is also reduced.

[0068]

Figure 14 is a block diagram showing a configuration of two dots multi-valued/dot phase weighting circuit, a second embodiment of the present invention. It is configured as provided with comparator 1401 instead of separator 1107 in two dots multi-valued circuit shown in Figure 11. Other parts are denoted as the same reference numerals as those in Figure 11.

[0069]

In a block diagram of two dots multi-valued circuit shown in Figure 11, comparison is made with two dots, six-bit each, reading data and density generating dot is switched for each pixel. A threshold for comparison is set and if data difference is within the threshold, density generating

dots are regularly arranged. On the other hand, in two dots multi-valued circuit shown in Figure 14, the high-order two bits from six bits of reading data is input into comparator 1401 as comparison data, and as a result of comparison, density is generated based on high reading density dots in the same way as the above description. Accordingly, comparison is made without regard of data spread of lower four bits of the reading data and the same effect as in the case when a threshold is provided for comparison can be obtained.

[0070]

In an exemplary circuit shown in Figure 14, the high-order two bits from six bits of reading data are assumed comparison data, several bits of reading data (from 1 to "reading data bit number" - 1) can be fixed or set arbitrary according to an image forming system. When the number of bits of comparison data decreases, a tendency toward a line image shown in Figure 15 is stronger as in the case that a threshold for comparison increases in the above-mentioned embodiment. This improves high quality reproduction of photo image. On the other hand, increasing of the number of bits of comparison data is effective for improving resolution in a text or a line image.

Figure 9

#1 OPTICAL WRITING METHOD

#2 ONE DOT

#3 OPTICAL OUTPUT

#4 MAIN SCANNING DIRECTION

#5 COUNTER SCANNING DIRECTION

(a) 1 × 2 MATRIX

(b) 2 × 1 MATRIX

Figure 10

(a) 1 × 2 MATRIX

(b) 2 × 1 MATRIX

(c) 1 × 2 MATRIX PHASE CONVERSION

(d) 2 × 1 MATRIX PHASE CONVERSION

Figure 11

#1 BLOCK DIAGRAM OF TWO DOTS MULTI-VALUED/DOT PHASE WEIGHTING CIRCUIT

#2 SCANNER I/F

1105 ADDER

1107 SUBTRACTING COMPARATOR

#3 PRINTER I/F

Figure 12

#1 TWO DOTS MULTI-VALUED γ CONVERSION TABLE

#2 OUTPUT

#3 INPUT

#4 BLACK

#5 WHITE

Figure 13

#1 WRITING IN TWO DOTS MULTI-VALUED METHOD

(1) MANUSCRIPT

(2) CONVENTIONAL METHOD

(3) PRESENT INVENTION

#2 MAIN SCANNING DIRECTION

#3 COUNTER SCANNING DIRECTION

#4 ONE DOT

#5 ONE PIXEL

Figure 14

#1 BLOCK DIAGRAM OF TWO DOTS MULTI-VALUED/DOT PHASE WEIGHTING CIRCUIT

#2 SCANNER I/F

1105 ADDER

1401 COMPARATOR

#3 PRINTER I/F

Figure 15

#1 TWO DOTS MULTI-VALUED DOT FORMING METHOD (CONVENTIONAL)

(a) 1 × 2 MATRIX

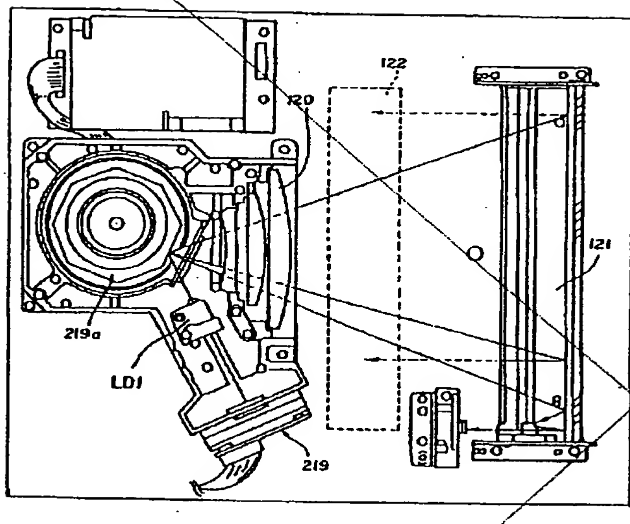
(b) 2 × 1 MATRIX

#2 MAIN SCANNING DIRECTION

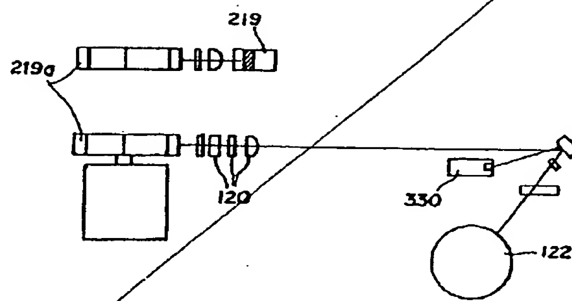
#3 COUNTER SCANNING DIRECTION

#4 ONE DOT

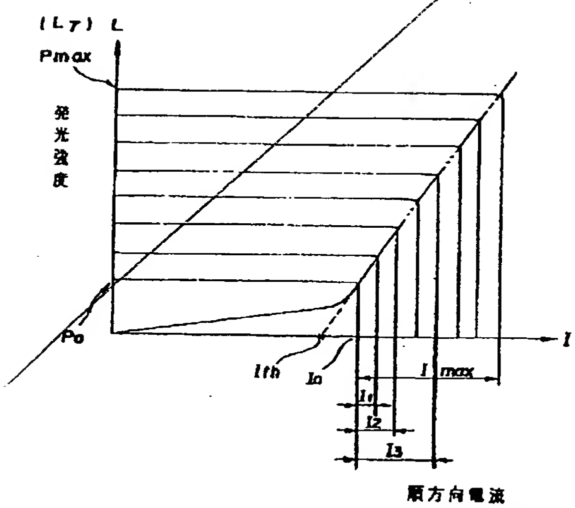
【図2】



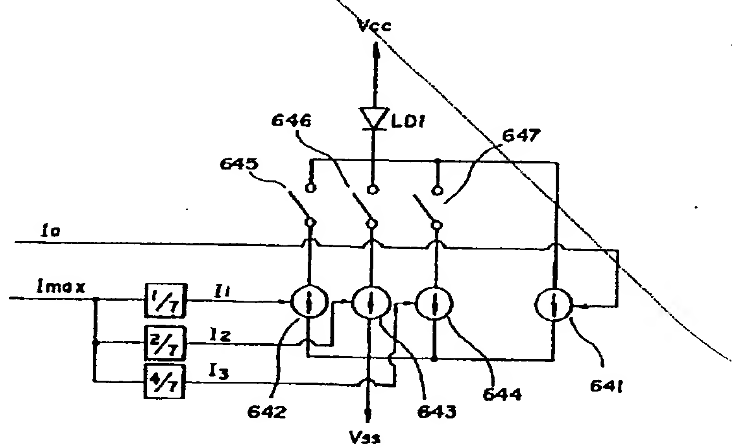
【図3】



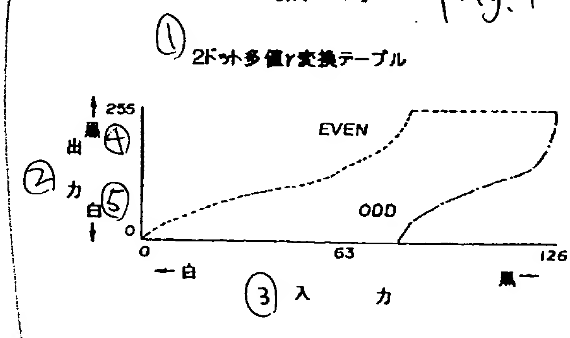
【図5】



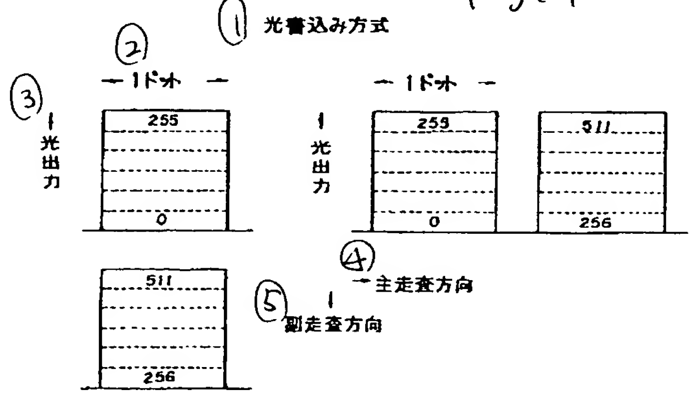
【図6】



【図12】 Fig. 12

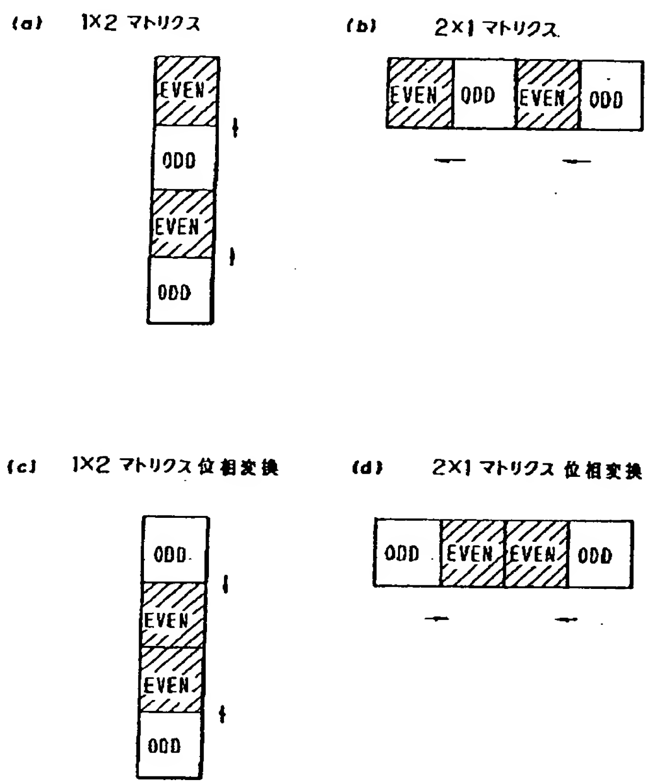


【図9】 Fig. 9



(a) 1X2 マトリクス　　　　(b) 2X1 マトリクス

【図１０】 Fig. 10



【図１３】 Fig. 13

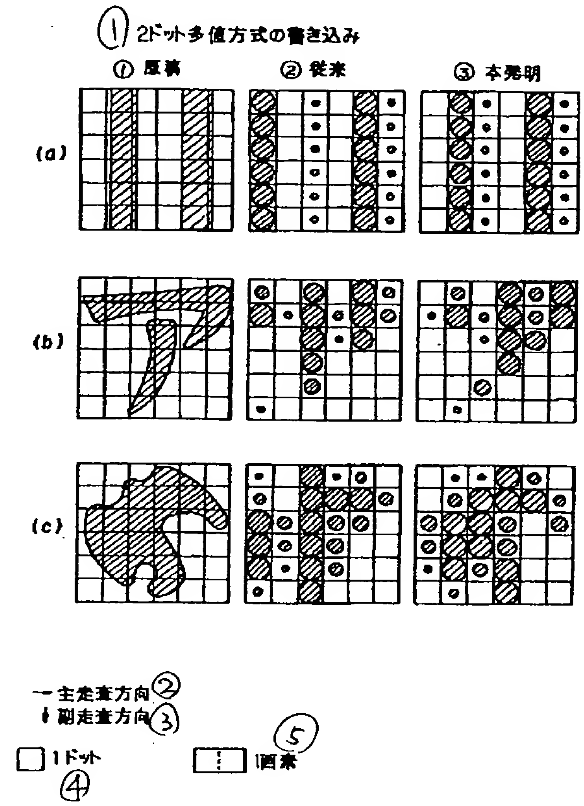
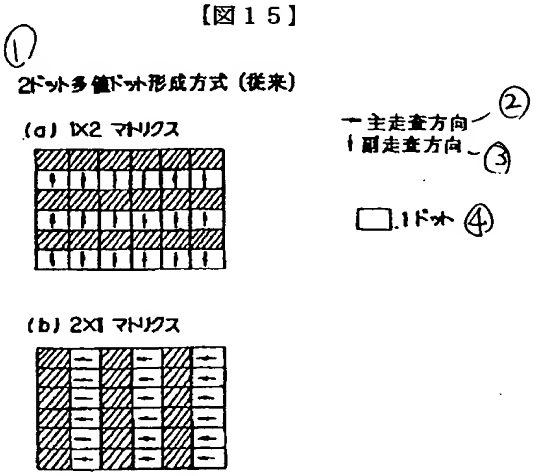


Fig. 15

【図１５】



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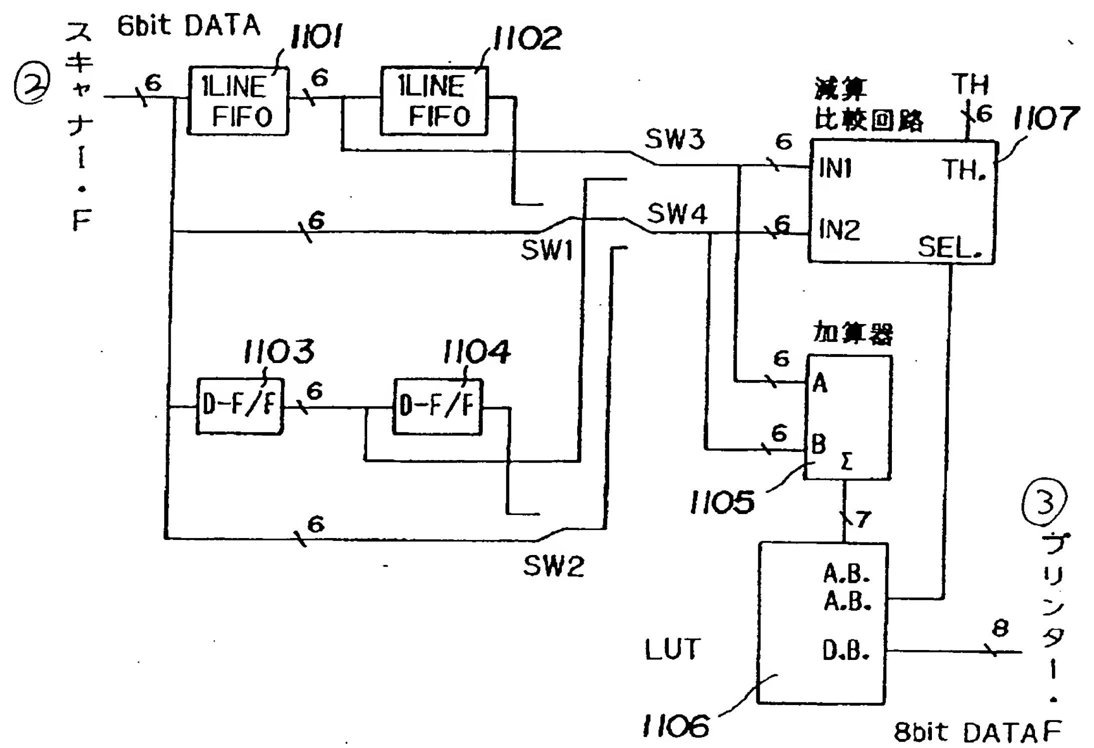
【図11】

Fig. 11

① 2ドット多値ドット位相重み付け回路ブロック図



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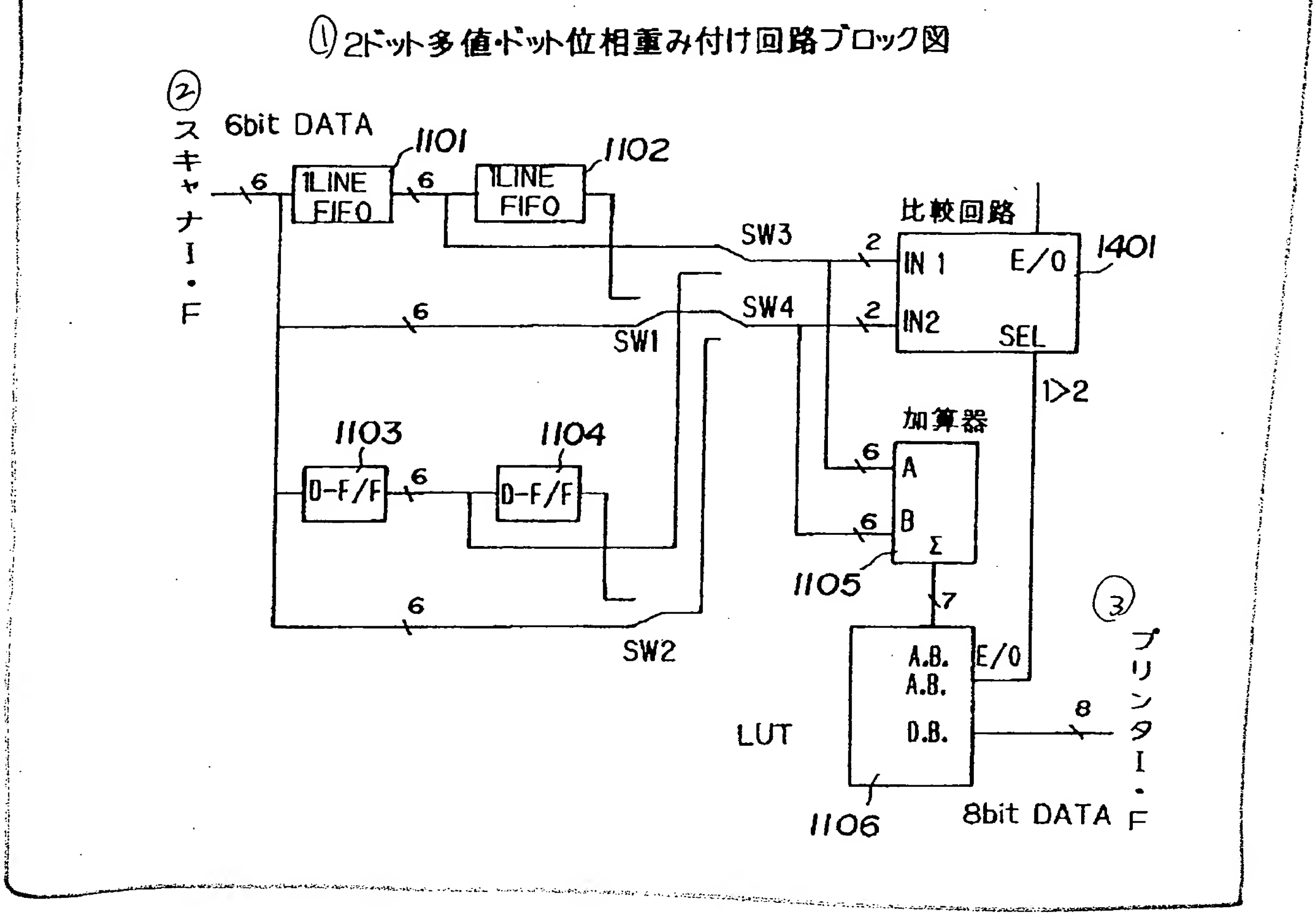
【図１４】　Fig. 14



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